Kindly **ADD** the following claims:

--180. An integrated circuit device comprising:

input receiver circuitry to sample an operation code synchronously with respect to a first transition of the external clock signal;

output driver circuitry to output data in response to the operation code specifying a read operation, wherein:

the output driver circuitry outputs a first portion of data in response to a rising edge transition of the first external clock signal; and

the output driver circuitry outputs a second portion of data in response to a falling edge transition of the first external clock signal.

181. The integrated circuit device of claim 180 further including a memory array having a plurality of memory cells.

182. The integrated circuit device of claim 181 wherein the input receiver circuitry receives address information synchronously with respect to the external clock signal.

183. The integrated circuit device of claim 182 wherein the input receiver circuit samples the address information synchronously with respect to a second transition of the external clock signal.

184. The integrated circuit device of claim 182 wherein the operation code and the address information are included in a packet.

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185. The integrated circuit device of claim 180 further including a clock alignment circuit to receive the external clock signal.

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186. The integrated circuit device of claim 185 wherein the clock alignment circuit generates an internal clock signal, and the output driver circuitry outputs data in response to the internal clock signal.

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187. The integrated circuit device of claim 180 wherein both the rising and falling edge transitions of the first external clock signal include voltage swings of less than one volt.

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188. The integrated circuit device of claim 180 wherein the rising edge transition of the first external clock signal and the falling edge transition of the external clock signal transpire in one clock cycle of the first external clock signal.

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189. The integrated circuit device of claim 180 wherein the input receiver circuitry receives block size information synchronously with respect to the external clock signal, wherein the block size information indicates an amount of data to be output by the output driver circuitry.

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190. The integrated circuit device of claim 180 wherein the input receiver circuitry receives a value which is representative of a number of clock cycles of the external clock to transpire before the output drivers outputs data.